74HC273; 74HCT273

Octal D-type flip-flop with reset; positive-edge trigger

Product data sheet

1. General description

The 74HC273; 74HCT273 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC273; 74HCT273 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (pin CP) and master reset (pin $\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

2. Features

- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC273						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	V_{CC} = 5 V; C_L = 15 pF	-	15	-	ns
t_{PHL}	HIGH-to-LOW propagation delay $\overline{MR}$ to Qn	V_{CC} = 5 V; C_L = 15 pF	-	15	-	ns
f_{max}	maximum input clock frequency	V_{CC} = 5 V; C_L = 15 pF	-	66	-	MHz

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Table 1: Quick reference data *...continued*

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_i	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to V_{CC}	[1]	-	20	-	pF
74HCT273							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	V_{CC} = 5 V; C_L = 15 pF		-	15	-	ns
t_{PHL}	HIGH-to-LOW propagation delay $\overline{MR}$ to Qn	V_{CC} = 5 V; C_L = 15 pF		-	20	-	ns
f_{max}	maximum input clock frequency	V_{CC} = 5 V; C_L = 15 pF		-	36	-	MHz
C_i	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to (V_{CC} – 1.5 V)	[1]	-	23	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC273				
74HC273N	–40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HC273D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HC273DB	–40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HC273PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HC273BQ	–40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74HCT273				
74HCT273N	–40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT273D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

Table 3: Pin description *...continued*

Symbol	Pin	Description
Q5	15	flip-flop output 5
Q6	16	flip-flop output 6
D6	17	data input 6
D7	18	data input 7
Q7	19	flip-flop output 7
V_{CC}	20	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating modes	Control		Input	Output
	$\overline{MR}$	CP	Dn	Qn
Reset (clear)	L	X	X	L
Load 1	H	↑	h	H
Load 0	H	↑	l	L

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
↑ = LOW-to-HIGH transition;
X = don't care.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = –0.5$ V to $(V_{CC} + 0.5$ V)	-	±25	mA
I_{CC}	quiescent supply current		-	50	mA
I_{GND}	ground current		-	–50	mA
T_{stg}	storage temperature		–65	+150	°C

Table 5: Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation					
	DIP20 package		[1]	-	750	mW
	SO20 package		[2]	-	500	mW
	SSOP20 package		[3]	-	500	mW
	TSSOP20 package		[3]	-	500	mW
	DHVQFN20 package		[4]	-	500	mW

[1] For DIP20 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO20 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP20 and TSSOP20 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN20 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC273						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r, t_f	input rise and fall time	V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
74HCT273						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r, t_f	input rise and fall time	V_{CC} = 4.5 V	-	6.0	500	ns

10. Static characteristics

Table 7: Static characteristics 74HC273

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V

Table 7: Static characteristics 74HC273 *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.5	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	µA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA

Table 7: Static characteristics 74HC273 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±5.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	µA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		I_O = −20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±10.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	µA

Table 8: Static characteristics 74HCT273

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = −20 µA	4.4	4.5	-	V
		I_O = −4.0 mA	3.98	4.32	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 µA	-	0	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	µA

Table 8: Static characteristics 74HCT273 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; I_O = 0 A	-	-	±0.5	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	µA
ΔI_{CC}	additional quiescent supply current	$V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
	pin $\overline{MR}$		-	100	360	µA
	pin CP		-	175	630	µA
	pin Dn		-	15	54	µA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = –20 µA	4.4	-	-	V
		I_O = –4.0 mA	3.84	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 µA	-	-	0.1	V
		I_O = 4.0 mA	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; I_O = 0 A	-	-	±5.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	80	µA
ΔI_{CC}	additional quiescent supply current	$V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
	pin $\overline{MR}$		-	-	450	µA
	pin CP		-	-	787.5	µA
	pin Dn		-	-	67.5	µA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = –20 µA	4.4	-	-	V
		I_O = –4.0 mA	3.7	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 µA	-	-	0.1	V
		I_O = 4.0 mA	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1.0	µA

Table 8: Static characteristics 74HCT273 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; I_O = 0 A	-	-	±10	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	160	µA
ΔI_{CC}	additional quiescent supply current	$V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
	pin $\overline{MR}$		-	-	490	µA
	pin CP		-	-	857.5	µA
	pin Dn		-	-	73.5	µA

11. Dynamic characteristics

Table 9: Dynamic characteristics 74HC273

Voltages are referenced to GND (ground = 0 V); $t_r = t_f$ = 6 ns; C_L = 50 pF unless otherwise specified; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 7				
		V_{CC} = 2.0 V	-	41	150	ns
		V_{CC} = 4.5 V	-	15	30	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	ns
		V_{CC} = 6.0 V	-	13	26	ns
t_{PHL}	HIGH-to-LOW propagation delay $\overline{MR}$ to Qn	see Figure 8				
		V_{CC} = 2.0 V	-	44	150	ns
		V_{CC} = 4.5 V	-	16	30	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	ns
		V_{CC} = 6.0 V	-	14	26	ns
t_{THL}, t_{TLH}	output transition time	see Figure 7				
		V_{CC} = 2.0 V	-	19	75	ns
		V_{CC} = 4.5 V	-	7	15	ns
		V_{CC} = 6.0 V	-	6	13	ns
t_W	pulse width					
	clock HIGH or LOW	see Figure 7				
		V_{CC} = 2.0 V	80	14	-	ns
		V_{CC} = 4.5 V	16	5	-	ns
		V_{CC} = 6.0 V	14	4	-	ns
	master reset LOW	see Figure 8				
		V_{CC} = 2.0 V	60	17	-	ns
		V_{CC} = 4.5 V	12	6	-	ns
		V_{CC} = 6.0 V	10	5	-	ns

Table 9: Dynamic characteristics 74HC273 *...continued*

Voltages are referenced to GND (ground = 0 V); $t_r = t_f$ = 6 ns; C_L = 50 pF unless otherwise specified; for test circuit see Figure 10.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rec}	recovery time $\overline{MR}$ to CP	see Figure 8					
		V_{CC} = 2.0 V		+50	–6	-	ns
		V_{CC} = 4.5 V		+10	–2	-	ns
		V_{CC} = 6.0 V		+9	–2	-	ns
t_{su}	set-up time Dn to CP	see Figure 9					
		V_{CC} = 2.0 V		60	11	-	ns
		V_{CC} = 4.5 V		12	4	-	ns
		V_{CC} = 6.0 V		10	3	-	ns
t_h	hold time Dn to CP	see Figure 9					
		V_{CC} = 2.0 V		+3	–6	-	ns
		V_{CC} = 4.5 V		+3	–2	-	ns
		V_{CC} = 6.0 V		+3	–2	-	ns
f_{max}	maximum input clock frequency	see Figure 7					
		V_{CC} = 2.0 V		6.0	20.6	-	MHz
		V_{CC} = 4.5 V		30	103	-	MHz
		V_{CC} = 5 V; C_L = 15 pF		-	66	-	MHz
		V_{CC} = 6.0 V		35	122	-	MHz
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to V_{CC}	[1]	-	20	-	pF
T_{amb} = –40 °C to +85 °C							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 7					
		V_{CC} = 2.0 V		-	-	185	ns
		V_{CC} = 4.5 V		-	-	37	ns
		V_{CC} = 6.0 V		-	-	31	ns
t_{PHL}	HIGH-to-LOW propagation delay $\overline{MR}$ to Qn	see Figure 8					
		V_{CC} = 2.0 V		-	-	185	ns
		V_{CC} = 4.5 V		-	-	37	ns
		V_{CC} = 6.0 V		-	-	31	ns
t_{THL}, t_{TLH}	output transition time	see Figure 7					
		V_{CC} = 2.0 V		-	-	95	ns
		V_{CC} = 4.5 V		-	-	19	ns
		V_{CC} = 6.0 V		-	-	15	ns
t_W	pulse width						
	clock HIGH or LOW	see Figure 7					
		V_{CC} = 2.0 V		100	-	-	ns
		V_{CC} = 4.5 V		20	-	-	ns
		V_{CC} = 6.0 V		17	-	-	ns
	master reset LOW	see Figure 8					
		V_{CC} = 2.0 V		75	-	-	ns
		V_{CC} = 4.5 V		15	-	-	ns
		V_{CC} = 6.0 V		13	-	-	ns

Table 9: Dynamic characteristics 74HC273 *...continued*

Voltages are referenced to GND (ground = 0 V); $t_r = t_f$ = 6 ns; C_L = 50 pF unless otherwise specified; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rec}	recovery time $\overline{MR}$ to CP	see Figure 8				
		V_{CC} = 2.0 V	65	-	-	ns
		V_{CC} = 4.5 V	13	-	-	ns
		V_{CC} = 6.0 V	11	-	-	ns
t_{su}	set-up time Dn to CP	see Figure 9				
		V_{CC} = 2.0 V	75	-	-	ns
		V_{CC} = 4.5 V	15	-	-	ns
		V_{CC} = 6.0 V	13	-	-	ns
t_h	hold time Dn to CP	see Figure 9				
		V_{CC} = 2.0 V	3	-	-	ns
		V_{CC} = 4.5 V	3	-	-	ns
		V_{CC} = 6.0 V	3	-	-	ns
f_{max}	maximum input clock frequency	see Figure 7				
		V_{CC} = 2.0 V	4.8	-	-	MHz
		V_{CC} = 4.5 V	24	-	-	MHz
		V_{CC} = 6.0 V	28	-	-	MHz
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 7				
		V_{CC} = 2.0 V	-	-	225	ns
		V_{CC} = 4.5 V	-	-	45	ns
		V_{CC} = 6.0 V	-	-	38	ns
t_{PHL}	HIGH-to-LOW propagation delay $\overline{MR}$ to Qn	see Figure 8				
		V_{CC} = 2.0 V	-	-	225	ns
		V_{CC} = 4.5 V	-	-	45	ns
		V_{CC} = 6.0 V	-	-	38	ns
t_{THL}, t_{TLH}	output transition time	see Figure 7				
		V_{CC} = 2.0 V	-	-	110	ns
		V_{CC} = 4.5 V	-	-	22	ns
		V_{CC} = 6.0 V	-	-	19	ns
t_W	pulse width					
	clock HIGH or LOW	see Figure 7				
		V_{CC} = 2.0 V	120	-	-	ns
		V_{CC} = 4.5 V	24	-	-	ns
		V_{CC} = 6.0 V	20	-	-	ns
	master reset LOW	see Figure 8				
		V_{CC} = 2.0 V	90	-	-	ns
		V_{CC} = 4.5 V	18	-	-	ns
		V_{CC} = 6.0 V	15	-	-	ns

Table 9: Dynamic characteristics 74HC273 *...continued*

Voltages are referenced to GND (ground = 0 V); $t_r = t_f$ = 6 ns; C_L = 50 pF unless otherwise specified; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rec}	recovery time $\overline{MR}$ to CP	see Figure 8				
		V_{CC} = 2.0 V	75	-	-	ns
		V_{CC} = 4.5 V	15	-	-	ns
		V_{CC} = 6.0 V	13	-	-	ns
t_{su}	set-up time Dn to CP	see Figure 9				
		V_{CC} = 2.0 V	90	-	-	ns
		V_{CC} = 4.5 V	18	-	-	ns
		V_{CC} = 6.0 V	15	-	-	ns
t_h	hold time Dn to CP	see Figure 9				
		V_{CC} = 2.0 V	3	-	-	ns
		V_{CC} = 4.5 V	3	-	-	ns
		V_{CC} = 6.0 V	3	-	-	ns
f_{max}	maximum input clock frequency	see Figure 7				
		V_{CC} = 2.0 V	4.0	-	-	MHz
		V_{CC} = 4.5 V	20	-	-	MHz
		V_{CC} = 6.0 V	24	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Table 10: Dynamic characteristics 74HCT273

Voltages are referenced to GND (ground = 0 V); $t_r = t_f$ = 6 ns; C_L = 50 pF unless otherwise specified; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 7				
		V_{CC} = 4.5 V	-	16	30	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	ns
t_{PHL}	HIGH-to-LOW propagation delay $\overline{MR}$ to Qn	see Figure 8				
		V_{CC} = 4.5 V	-	23	34	ns
		V_{CC} = 5 V; C_L = 15 pF	-	20	-	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; see Figure 7	-	7	15	ns
t_W	pulse width					
	clock HIGH or LOW	V_{CC} = 4.5 V; see Figure 7	16	9	-	ns
	master reset LOW	V_{CC} = 4.5 V; see Figure 8	16	8	-	ns

Table 10: Dynamic characteristics 74HCT273 *...continued*

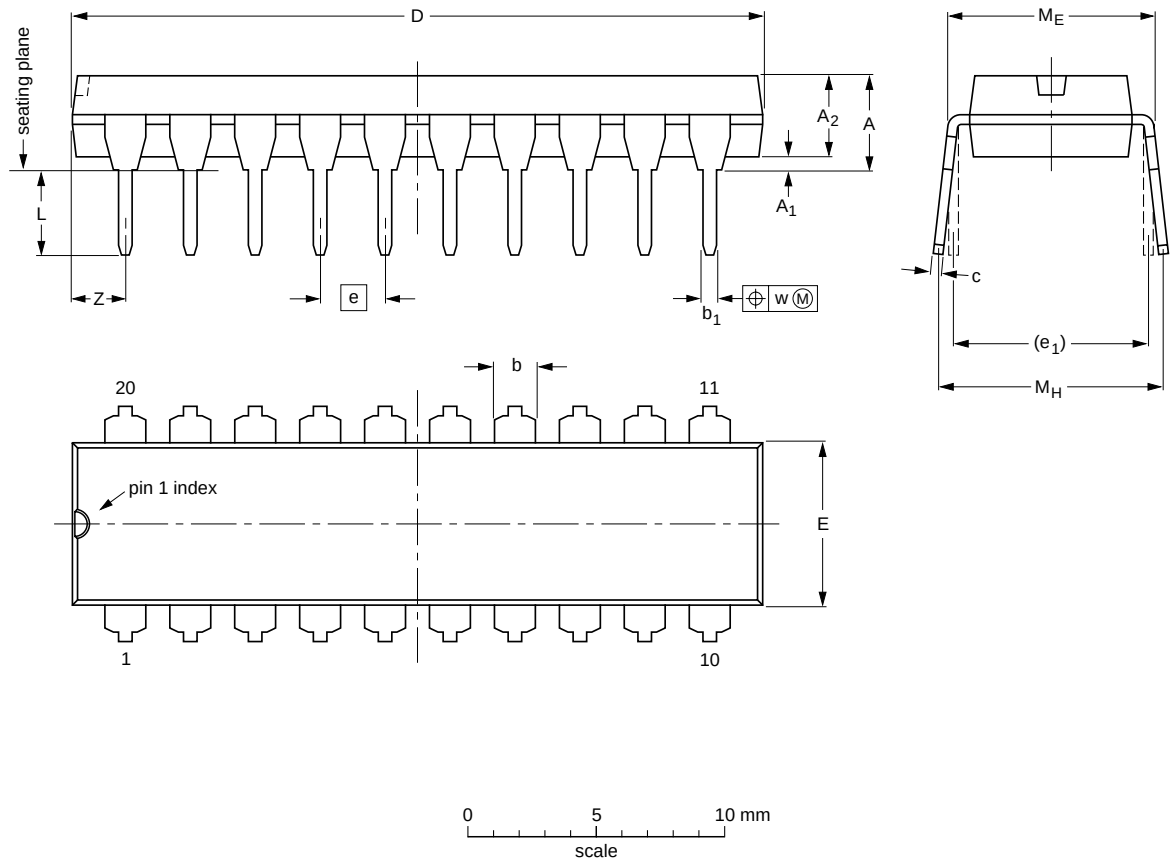
Voltages are referenced to GND (ground = 0 V); $t_r = t_f$ = 6 ns; C_L = 50 pF unless otherwise specified; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rec}	recovery time $\overline{MR}$ to CP	V_{CC} = 4.5 V; see Figure 8	+10	–2	-	ns
t_{su}	set-up time Dn to CP	V_{CC} = 4.5 V; see Figure 9	12	5	-	ns
t_h	hold time Dn to CP	V_{CC} = 4.5 V; see Figure 9	+3	–4	-	ns
f_{max}	maximum input clock frequency	see Figure 7				
		V_{CC} = 4.5 V	30	56	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	36	-	MHz
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to (V_{CC} – 1.5 V) [1]	-	23	-	pF
T_{amb} = –40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	V_{CC} = 4.5 V; see Figure 7	-	-	38	ns
t_{PHL}	HIGH-to-LOW propagation delay $\overline{MR}$ to Qn	V_{CC} = 4.5 V; see Figure 8	-	-	43	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; see Figure 7	-	-	19	ns
t_W	pulse width					
	clock HIGH or LOW	V_{CC} = 4.5 V; see Figure 7	20	-	-	ns
	master reset LOW	V_{CC} = 4.5 V; see Figure 8	20	-	-	ns
t_{rec}	recovery time $\overline{MR}$ to CP	V_{CC} = 4.5 V; see Figure 8	13	-	-	ns
t_{su}	set-up time Dn to CP	V_{CC} = 4.5 V; see Figure 9	15	-	-	ns
t_h	hold time Dn to CP	V_{CC} = 4.5 V; see Figure 9	3	-	-	ns
f_{max}	maximum input clock frequency	V_{CC} = 4.5 V; see Figure 7	24	-	-	MHz
T_{amb} = –40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	V_{CC} = 4.5 V; see Figure 7	-	-	45	ns
t_{PHL}	HIGH-to-LOW propagation delay $\overline{MR}$ to Qn	V_{CC} = 4.5 V; see Figure 8	-	-	51	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; see Figure 7	-	-	22	ns
t_W	pulse width					
	clock HIGH or LOW	V_{CC} = 4.5 V; see Figure 7	24	-	-	ns
	master reset LOW	V_{CC} = 4.5 V; see Figure 8	24	-	-	ns
t_{rec}	recovery time $\overline{MR}$ to CP	V_{CC} = 4.5 V; see Figure 8	15	-	-	ns
t_{su}	set-up time Dn to CP	V_{CC} = 4.5 V; see Figure 9	18	-	-	ns
t_h	hold time Dn to CP	V_{CC} = 4.5 V; see Figure 9	3	-	-	ns
f_{max}	maximum input clock frequency	V_{CC} = 4.5 V; see Figure 7	20	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;

13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			

Fig 11. Package outline SOT146-1 (DIP20)